# Project description:

## Background

### State of the art:

One of the hottest topics in condensed matter physics is the realization of a quantum computer. The main advantage of such a quantum computer would be its ability to solve specific classes of algorithms orders of magnitudes faster than classical computers.

As we all know a classical computer is based on deterministic two states called bits. A quantum computer is also based on two level states (basis states) called quantum bits (qubits). However, a qubit unlike q classical bit exploits the quantum effect of superposition. As a consequence, a quantum system can be simultaneously in both basis states.

There have been several proposals for implementing such a qubit (just solid state implementations are listed below):

* Electrons on Helium (He) [1]
* Semiconductors:
  + - Nuclear spin qubits [2]
    - Electron (hole) spin qubits [3]
* Superconductors:
  + - Flux qubits [4]
    - Charge qubits [5]

As stated above, one of the suggestions, which came in 1998 by Loss and DiVincenzo, was to use the spin of electrons (holes) for the realization of qubits. The spin is an intrinsic quantum mechanical property of every elementary particle. In a magnetic field the spin degree of freedom lifts the degeneracy of an orbital energy level. The level splits into two, typically labelled as spin-up and spin-down. This two level system can act as a qubit, the so-called spin qubit.

However, for accessing and manipulating the spin degree of freedom, one must first confine the charge into a region, which is in size comparable to the charge particle wavelength. Such a confinement can take place in a so-called quantum dot (QD). QDs are very small structures (their diameters can reach tens of nanometers) and because of their almost zero dimensionality, the energy levels for a charge particle are discrete and far away from each other. By applying external magnetic field spin energy states splits in two and become distinguishable for manipulation and readout. A few years after the Loss-DiVincenzo proposal for the realization of a scalable quantum computer, DiVincenzo published a list of conditions which a qubit should fullfill for a quantum computer to work correctly [6]:

The 5 criteria for quantum computation are:

* **Identification of well-defined qubits:** A well defined qubit is a two level (two state) system whose levels are distinguishable and highly controllable. The qubit operation takes place by operating (manipulating) this two states.**Reliable state preparation:** To be able to always deterministically drive the qubit into the initial state so it is ready for the next computation.
* **Low decoherence times (long coherence times):** Because of the several noise sources coupled to the qubit its initially prepared state is lost (decohered) with the time. It is desirable to have coherence time as long as possible.
* **Accurate quantum gate operations (state manipulation):** As it is known, in a classical logic operators (gates), the input states (voltage levels) act on the transistors switching them on or off and thus determine an output state (voltage level). Quantum logic gate state is represented by the qubits spin directions. Gate operation in the quantum logic consist of rotations of this spins around different (operation defined) axes, for the operation defined angles. Rotations are usually achieved by means pulses which duration define rotation angles and it needs to be very accurate.
* **Strong quantum measurements (state readout):** Quantum measurement is a projection of a qubit spin vector from a calculation determined position (qubit state) to the basis state axes and obtaining the result as up or down (state readout).

**In all spin qubit approaches above (and all qubits in overall) there is battle between the spin manipulation time on one side and the coherence time on the other side. For making a set of quantum operation correctly, the manipulation time for one operation need to be much shorter than the coherence time. Benchmark for the manipulation time is minimum time needed for one full spin rotation (π pulse), τπ.**

**Materials**

Silicon **(Si)** has emerged as a promising material for the spin qubits because it can be isotopically purified and left just with the 28Si isotope which is a nuclear spin zero element. Thus the nuclear noise can be eliminated and the coherence time boosted in comparison to the broadly used gallium arsenide (GaAs) in a spin qubit community today. The additional big advantage is its compatibility with current CMOS technology. This could become very important when moving towards the realization of a large number of qubits as required by quantum algorithms.

(speak about the three types of Si quantum dots dzurak, Eriksson,, heterostructures, Morello and what Simmons does with STM. In this discussion it needs also to come out that geometries are getting more and more complex there are people fabrication quintuple dots) There are several approaches of defining quantum dots in silicon, in which qubits are achieved at the moment.

One way is by means of a phosphorous P doping in the specific Si crystal regions. In that case a phosphorous atom behaves as an electron quantum dot because of its confining potential. Andrea Morello’s Group from the UNSW in Australia, by applying the Hahn echo pulse sequence, has measured the electron spin coherence time T2 exceeding 200 microseconds, in a non – isotopically purified Si:P system, while the duration of π pulse in this case τπ = 75 ns [3]. By using the isotopically purified 28Si:P and the nuclear spin of phosphorous atom as a qubit, the same group has achieved nuclear spin coherence time of 60 milliseconds and duration of the π pulse of around τπ = 50 μs [2].

M. Veldhorst et al. by using lithographical definition of electron quantum dots in silicon has measured spin coherence time using CPMG pulsing technique T2CPMG = 28 ms and the π pulse duration time for that case is τπ = 1.5 μs [17].

E. Kawakami et al. by using the single-electron quantum dot in the Si/SiGe heterostructure with two layers of the electrostatic gates as a qubit, has measured the coherence time using the Hahn-echo pulse sequence T2 = 40 μs. Spin flip duration is around τπ = 0.15 μs, extracted from supplementary information [18].

The major drawback in silicon is the relatively weak spin orbit coupling for electrons which results in difficult spin manipulation via electric fields (as described in more detail in *The spin manipulation measurements*). One solution around this problem is to use holes instead of electrons.

Using hole spin in p-type silicon industrial CMOS as qubit basis, R. Maurand from S. De Franceschi group in CEA Grenoble, achieved π spin rotation time of approximately τπ = 3 ns. While coherence time using Hahn echo pulsing sequence T2 in their case was 245 ns [11].

Holes in germanium **Ge**, on the other hand, have much higher spin orbit coupling which should lead to much **faster spin manipulation time**.

Another other way for defining QDs on a silicon based platform, used in our group, is by combining it with germanium Ge [10].The epitaxial growth of Ge on Si can lead to the formation of QDs and and hut wires (a special type of nanowires) due to the different lattice constant between them. Recently magnetotransport measurement have shown that holes, in this type of structures, are of the **heavy hole type** what leads to the **longer** dephasing and thus longer **coherence times**.



Figure 1: Scanning electron micrograph of SiGe nanowire contacted by palladium Pd source and drain electrodes [10]

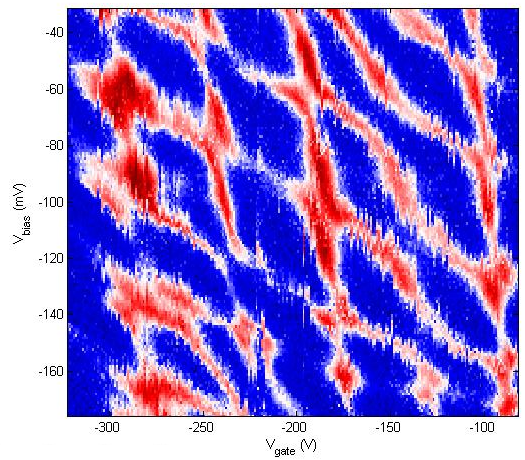


Figure 2: Stability diagram of a SiGe nanowire double quantum dot

Scale up demand of a quantum computation requires qubit coupling. Spin qubit community is trying to reply on that with several approaches: From C. M. Marcus and Quantum Transport laboratory in Delft – triple quantum dots. From D. J. Reilly laboratory - quadruple-quantum-dot. From S. Tarucha laboratory - quintuple quantum dot.

Different type of measurement techniques are applied in order to measure the state of a spin qubit and extract the coherence times:

* DC current readout
* Differential measurement (AC current readout)
* Ohmic reflectometry
* Gate reflectometry

The DC current readout is sensing the electron transport through the qubit by means of current measurement. It is prone to low frequency 1/f noise and BW is low because of heavy filtering for achieving low effective electron temperatures.

Differential measurement (AC current readout) has the same drawbacks as DC current readout. It is typically done with low frequency lock in technique. Because of the low frequency noise, lock in amplifier usually operates on very narrow bandwidth around frequency of the measurement sinusoidal signal, which lead to long measurement time.

Ohmic reflectometry is a technique of indirect qubit impedance change sensing by monitoring the amplitude or phase of the wave reflected from the qubit (see Figure 3 for a more detailed explanation). It is usually done by high frequency lock in techniques and is not prone to 1/f noise.

Finally, gate reflectometry is a technique of indirect sensing of the change in the qubit capacitance by monitoring the amplitude or phase of the portion of the sent wave reflected from the one of the qubit gates. **It’s big advantage is that it does neither require charge transport through the qubit nor the existence of a no charge sensor.**

**What is reflectometry?**

**C:\Users\jkukucka\Documents\GitHub\Fellowship\Reflectometry_basics.tif**

Figure 3: Basic principle of ohmic reflectometry. CS and RS constitutes the equivalent electrical schematic of a measured sample, e.g. a single hole transistor (SHT) formed by the single quantum dot. S and D denotes source and drain contacts of the single SHT, respectively. The resonance circuit formed with an inductor L and a capacitance C is connected to the source contact.

Reflectometry is a readout technique based on the change of the wave reflection coefficient Γ. It comes from the electromagnetic wave principle – if a wave is travelling in a media with impedance Z0  (e.g. coax cable) and it encounters a change of impedance (e.g. coax end) to Z, a portion of the wave will be reflected back according to the expression: , where Ar is amplitude of a reflected, Ain amplitude of an incoming wave and Γ is reflection coefficient.

By putting a resonant circuit connected to a single hole transitor (Figure 3, red polygon) instead of coax cable end one can measure its impedance change due to a hole tunneling. If elements of a resonant circuit, inductance L and capacitance C are properly chosen, on the resonant frequency of that circuit, , wave reflection coefficient Γ is minimized. Proper choosing means that the impedance of complete matching circuit on resonance is equal, or matches, characteristic impedance of the coax line Z0. Thus if a hole tunnels -> the single hole transistor (SHT) impedance changes -> reflection coefficient changes -> amplitude and phase of the reflection wave changes.

### Definition of the problem:

As mentioned before DQD are defined by gates positioned on top of the nanowire (Figure 2). Static voltage on gates G1 and G2 create the potential wells forming the double quantum dot system. For operating this DQD as a qubit it needs to be isolated from the ohmic contacts, which can be achieved by G3 and G5.

**Since the charge transport through the DQD is forbidden, all readout techniques based on charge transport are not applicable since no current is flowing through the device. (I doubt that you would be able to see sth even if you integrate long enough. How long would you need to integrate to see a let’s say 0.1fA current signal?). Readout techniques in this category are DC current readout, AC current readout and ohmic reflectometry.**

A usual solution to this problem is to place next to the DQD an additional, separated quantum dot in the form of a single electron (hole) transistor or quantum point contact, called charge sensor (Figure 1). The charge sensor is electrostatically coupled and thus sensitive to the charge configuration in the DQD. The charge sensor itself is well coupled to ohmic contacts thus it is suitable for charge transport measurements and ohmic reflectometry.

**However, charge sensors suffer from conductance profile thermal broadening what lowers the sensitivity thus speed of readout. They also need additional compensation gates to substract the influence of the qubit gates on their conductance. Also, by looking into the future, for the realizatioin of a usable quantum processor, the qubit number needs to be drastically scaled up to achieve a large enough number as required by quantum algorithms.** **Gate reflectometry does not suffer from previously listed problems and since it is using already defined electrostatic gates it does not need a charge sensor, thus has a big potential to address the scalability problem. Furthermore,** by using frequency division multiplexing, all qubits in a quantum processor could be read out through a one (or several) wires. (Should you discuss here frequency crowding? What does the difference in resonant frequencies need to be?)

I think you should start with the work of Reilly and some other groups and then say what is the work with the highest achieved sensitivity sofar. Last year, M.F. Gonzalez – Zalba et al. reported a charge sensitivity of 37 μeHz-1/2 by using gate reflectometry for silicon nanowire based DQD device [12]. The reported sensitivity is similar to that achieved with ohmic reflectometry in charge sensors (RF quantum point contact and RF single electron transistor) which is in μeHz-1/2 regime [12], but suffers from all the issues stated above.

### Proposal objectives:

The objectives of this proposal are to design a **fast gate reflectometry** system which will be used in order to study the LD qubit created in a a germanium based, double quantum dot.

For the gate reflectometry, the goal is to achieve a charge sensitivity comparable or even faster than that reported in [12]. Such would allow us to have a high bandwidth system necessary for the qubit read out (do you wanted to say sth different?) After the gate reflectometry set up will have been set up the focus will go to the realization of the LD hole qubit in a DQD structure. The first measurements to be performed are the ones for determining the spin relaxation time T1. the time during which the spin stays in the excited state before relaxing to the ground state. Subsequently experiments in order to investigate the coherence time of the qubit are going to be performed. More concretely, spin manipulation experiments for measuring the spin dephasing time T2\*, the spin coherence time using Hahn echo technique T2, and the spin coherence time using the CPMG pulse sequence technique T2 CPMG, are going to be conducted.

### Working schedule:

#### Designing initial version of reflectometry setup: sample holder, readout circuit, instrumentation setup

**Sample holder**

One of the key measurement requirements is to lower the electron thermal energy to be able to resolve energy level splitting needed for confining one charge particle spin (what do you mean by this?). For that reason it needs to be cooled down to low temperatures. In this case it is 4 Kelvin (K) or below. For the initial version of measurement system 4 K dewar with liquid helium has been used.

Why don’t you start with sth like. In order to tune the gate reflectometry system measurements will be initially performed at 4k. Such temperatures are needed for…. During the first year of my PhD I have already prepared a 4K dip stick for such reflectometry measurements (then you can describe the stick). I would not now go into double quantum dots. When you will characterized the gate reflectometry initially you will start with single quantum dots and then you move towards double quantum dots.

Double quantum dots samples are grown on silicon wafers and then cutted in 5x5 mm pieces. They need to be dipped into the liquid helium dewar for cooling. For this purpose Plexiglas sticks (Figure 5), were used. The sample can be positioned on the top of the stick on the so called sample holder. Since, electrical signals needs to be delivered and afterwards measured from the sample, the sample holder is done as printed circuit board (PCB) which routes all the electrical signals to and from the sample. From the room temperature instruments, DC electrical signals are sent through the low thermal conductive twisted pair wires finishing in a PCB connector and radio frequency signals are sent through coaxial cables. Going from PCB DC connector, DC signals are low pass filtered with sourface mounted RC filters (Figure 4) to reduce thermal noise from the wires. After low pass filtering, DC signals are routed to the gold plated bonding pads around area in the middle of the PCB (sample area) on which a typically 5x5 mm sample is glued with silver paste (Figure 4). Electrical contacts from PCB bonding pads to on the sample bonding pads electrically connected to the DQD gates are achieved by wedge wire bonding technique. RF coaxial lines are finishing on the PCB mounted SMP connectors. After SMP connector, using bias tee, DC signal is added to the RF signal. From there signal is routed to the PCB bonding pads. SMP connectors and bias tees can be seen on Figure 4. Further these signals are connected to DQD gates with the same wedge wire bonding technique.

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Figure 4: Initial version of the PCB sample holder. The top figure show the upper view of the PCB board while the lower figure focuses on the back side.

**Readout circuit**

To measure the charge state of the nanowire single hole transistor (SHT), ohmic reflectometry technique was applied. For that purpose the RF signal was sent down the coax line (Figure 5, right). The reflected signal was separated in the directional coupler and directed to the Weinreb’s CITLF2 and Minicircuits ZX60-33LN-S+ amplifiers (Figure 5, right) to make the SNR immune to the next room temperature stages (explain a bit more). The amplitude of the reflected signal from the resonator circuit depends on the SHT charge state. The explanation of the working principle of ohmic reflectometry can be found at the end of the “State of the art” chapter. The used resonator circuit consisted of a matching circuit (Figure 4) and the SHT resistance RS in parallel to the parasitic capacitance CS, as can be seen in a simple circuit model in Figure 3. Finally there exists always a parasitic capacitance, which is a capacitance to the ground that comes from bonding wires, the sample itself, the RF line and the used inductor.

(*There is nice circuit schematic in the Natalia paper. Since she is not explicitly telling that lowering parasitic capacitance increases sensitivity, I was thinking, maybe it would be good to take that circuit model with a reference and make a simulation in Qucs showing that with lowering parasitics, change in reflection coef increases. For the purpose of justifying lowering parasitic capacitance by removing grounds in the PCB- This seems like a good idea!*)

For the purpose of minimization of this parasitic capacitance and thus increase sensitivity of the reflectometry, the PCB ground plane is removed below the RF lines, the corresponding PCB bonding pads and the sample.   
Matching circuit elements used are surface mounted inductor Murata 1,2 μH and varactor MACOM MA46H070-1056. A Varactor – a voltage tunable capacitor - was used to be able to always achieve good matching condition despite the change of the SHT resistance Rs following the approach in [13]. (Put this in reflectometry explanation and here just refer to it)Matching condition is situation in which large resistance (~100 KΩ) of the single hole transistor (SHT) is transformed to near 50 Ω value what is characteristic impedance of the RF line, thus minimizing reflected signal amplitude (as can be seen in the reflectometry explanation at the end of the “State of the art” chapter) (do we need to say it again?). For this case change in a reflected signal amplitude due to SHT charge configuration change is maximized and consequently measurement sensitivity is maximized [13].

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Figure 5: Plexiglas dip-stick used for cooling down samples mounted on the PCB to 4K. The left picture shows the whole, , while right is the zoom in, highlighting the directional coupler (up) and low noise Minicircuits ZX60-33LN-S+ RF amplifier (down). An additional low noise cryogenic RF amplifier CITLF2 from Sander Weinreb’s Caltech Microwave Research Group can be added in order to increase the SNR of the measured signal.

*I would add here the picture of your ohmic reflectometry measurement.*

*I should read up to here, right?*

**Instrumentation setup**

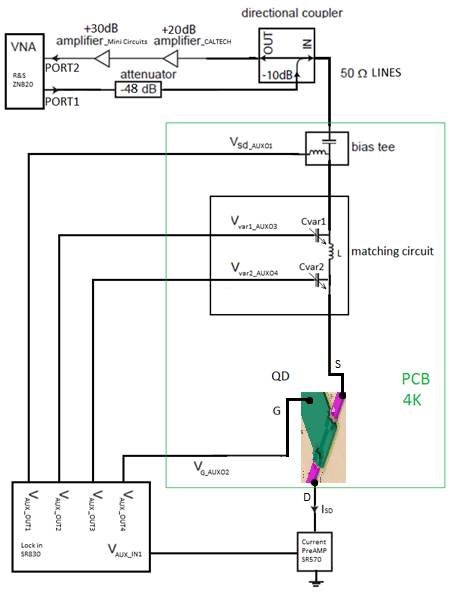


Figure 6: Simplified schematic of the overall measurement circuit

For conducting the measurements several instruments has been used. For measuring reflectometry signal (reflection coefficient) vector network analyzer (VNA) from Rohde and Schwarz, model ZNB20, has been used. For DC biasing of the single hole transistor, the auxiliary bias outputs of the Stanford Research SR830 lockin amplifier has been used. For DC current measurements current amplifier from Stanford Research SR570 has been used. For attenuating RF signal sent to the sample Minicircuit’s attenuator has been used and for amplifying RF signal reflected from the sample, series of Minicircuit’s and CITLF3 low noise amplifier has been used. Instrument control and data retrieval to the PC has been done using Python application.

#### Germanium nanowire based, hole spin single quantum dot tuning and characterization with initial version reflectometry setup



Figure 7: 3D model of silicon germanium nanowire based single quantum dot sample, designed by H. Watzinger. Hole spin single quantum dot is formed in the nanowire beneath the gate (green).

The single hole transistor (SHT) sample was fabricated by H. Watzinger and nanofabrication description can be found in [10].

Using setup described in previous chapter, the SHT formed as a single quantum dot in germanium nanowire (Figure 7) was tuned in the Coulomb blockade regime applying DC voltages on source, drain and gate electrodes (Figure 6). Charge stability measurements were conducted in the Coulomb blockade regime showing Coulomb diamond pattern, as in [10]. Comparison of DC current and ohmic reflectometry measurement has been done. DC current was measured applying bias on source and reading current from drain contact (Figure 6), while reflectometry LC matching circuit was connected to the SHT source contact (Figure 6).



Figure 8: Comparison of the DC current transport (left) and the ohmic reflectometry (right) mesurements of the SHT charge stability measurement.

Putting the integration time similar for both measurements, Figure 8 reveals that reflectometry technique enables us to see more features like the excited orbital energy states of the SHT.

#### Second generation of the reflectometry setup

The initial measurements have been done in a liquid helium at the 4 K temperature. Going lower in temperature, further decreases an electron effective temperature needed to resolve the physical effects in the next experiments.

Our group has changed the laboratory environment which is now placed at IST Austria. New lab is equipped with dilution fridges allowing us to achieve temperatures down to 10 mK.

For the purpose of measuring several samples and necessity for the higher number of RF lines dictated by next experiments of spin manipulation, the new PCB was designed (Figure 9). New design allows frequency multiplexing of four different reflectometry resonant circuits enabling measurement of four samples at once. Also, new type of the PCB holder (dilution fridge insert), replacement for the previously used Plexiglas stick was manufactured by dilution fridge company and equipped with coax cables, attenuators, cryogenic amplifier, directional coupler by our electronic technician Thomas Adletzberger to reproduce the reflectometry system mounted on the Plexiglas stick and upgrade. Upgrade is done is terms of using lower thermal conducting stainless steel and superconducting niobium titanium coaxial cables, attenuators, additional DC filtering of all DC wires. Niobium titanium cables are used between the input of the cryogenic amplifier and sample stage because of their very low thermal conduction, to avoid heating of the sample stage of the fridge which has cooling power in tens of uW.

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Figure 9: Newer version of the PCB (green) with the mounted sample (middle, grey) fabricated in our group by Lada Vukušić. Altogether mounted on the golden plated copper fork on the dilution fridge insert. The copper colored wires are the coaxial cables providing the high frequency connection for a spin manipulation and readout.

*Maybe I can put some nicer picture of PCB + PCB holder, we have some pretty, artistic like ones.  
Maybe put the some picture of the probe (currently I don’t have the nice one)*

Vector network analyzer used so far for the measurements is replaced with Zurich Instruments UHF lock in amplifier which enables faster and longer data acquisition, more inputs and generally more measurement flexibility. For the spin relaxation time and spin manipulation measurement arbitrary waveform microsecond pulses with a nanosecond rise time are needed. Those are generated using the Tektronix AWG5014C. Measurement is conducted using the QTLab measurement application developed in Python initially by Delft Quantum Transport (QT) laboratory. We modified it according to our need. All the codes can be found on the GitHub.

***TO DO:***

#### Moving to the gate reflectometry

Gate reflectometry readout parameters are phase shift ∆φ and amplitude change ∆γ of the reflected signal due to charge configuration change in the quantum dot or double quantum dot system. , , , where Q is the quality factor of the resonant circuit, Cp is parasitic capacitance, Cg is gate to dot coupling capacitance and CΣ is quantum dot overall capacitance [12]. From the above expressions it can be seen that higher dot to gate coupling Cg leads to higher sensitivity of both ∆φ and ∆γ. Since gate electrode and nanowire, with dielectric layer in between, forming approximately parallel plate capacitor structure . Using gate reflectometry in gate defined DQD in GaAs J.I. Colless et al achieved charge sensitivity of 6.3 meHz-1/2, having Cg/CΣ ≈ 0.05 [14]. Using 1.9 nm HfSiON oxide as dielectric in a silicon nanowire field effect transistor, M.F. Gonzalez – Zalba et al. achieved the charge sensitivity of 37 μeHz-1/2, with Cg/CΣ = 0.92 [12]. In our system using the HfO2 as a dielectric which has εroxide = 24 we can go down to 4 nm in thickness, so we expect to have Cg/CΣ comparable to [12].

*(Here it is maybe possible to put in Qucs simulation using circuit model similar to Natalia but adopted for gate reflectometry, to see how the quality factor of reflection parameter is changing with L and C.)*

From the equation for ∆φ, it seems that the roadmap for getting sensitive gate reflectometry, firstly is to reduce the parasitic capacitance as much as possible by engineering the sample holder, as described in the “Readout circuit” chapter. Secondly, to tune to the good matching condition by changing the inductor values in the resonant circuit.

**Second generation of the ohmic reflectometry** setup would be than adopted to the **first generation of the gate reflectometry setup** by **changing inductor values**, and by trying different inductors by means of core material and size in order to reduce inductor losses.

#### Optimizing the gate reflectometry:

There are several sources of the signal loss in the gate reflectometry system: inductor losses, PCB dielectric losses, losses in PCB RF transmission lines, losses caused by the geometric parasitic capacitance [12].

For **minimization of the geometric parasitic capacitance** coming from the coupling of the PCB RF lines and bonding pads to the ground planes, Sonnet software can be used. *(Maybe to put here – optimization based on Sonnet – Matlab (Octave) communication)*

The RF lines transmission losses come probably mainly from the unwanted reflections due to the transmission line routing and splitting needed to connect more reflectometry readout circuits – frequency multiplexing. This assumption should be tested and **optimum configuration of the PCB RF lines** could be achieved using Sonnet software for simulating RF line scattering parameters.

Inductor losses are dissipation on the ohmic resistance of the wire wound and core losses due to hysteresis and eddy currents. Overall loss can be represented as the inductor equivalent series resistance. Inductors with air core have smaller core losses but for achieving high inductor values they need to have more wounds and they are bigger, lowering their self – resonant frequency and increasing wire resistance. As a part of this work, **examination of the inductor influence** on the gate reflectometry sensitivity regarding the core material and the inductance value could be conducted.

Losses in the PCB dielectric could be addressed by using dielectric with lower dielectric loss then currently used FR4, e.g. some of the Rogers Corporation laminates.

#### Measuring the spin relaxation time T1

*(Explained for the spin ½ double dot qubit) (many of the stuff in this explanation are copied from your Marie Curie proposal)*

For measuring the spin relaxation time a three level pulse sequence will be used, similar to approach of Morello et al. [4]. The left dot is initially empty while the right dot is populated with a spin up hole. First, pulsing the gate of the left dot brings its spin up and spin down energy levels below the Fermi level, μF, of the lead. *(I am not sure here, weather for the holes Fermi energy need to be above or lower to allow tunneling)* Since the tunneling is most likely spin independent, the left dot is loaded with a random hole spin from the lead, during the loading time tL. The double dot is left in that configuration for the waiting time tw. After the tw, the second pulse level brings the higher energy spin down level of the left dot in the resonance with the empty spin down level of the right dot. If the spin down electron have been loaded to the left dot during the tL, it will tunnel to the right dot in the read phase, causing the shift in the quantum capacitance which is read by the gate reflectometry. Otherwise it will stay on the left dot, causing a zero gate reflectometry readout. The probability of finding the electron in the excited spin-down state will decay exponentially with the duration of the waiting time tw, with *T*1 being the decay constant.

#### The spin manipulation measurements

Quantum gate operation in a spin qubit assumes spin manipulation. Basically those manipulation are spin rotations in the spin representation sphere, called Bloch sphere.



Figure 10. Bloch sphere

Basis spin states in a hole spin qubit are spin up and spin down, laying on the z axes of the Bloch sphere. Their energy splitting EZ is determined by the hole g factor g, the Bohr magneton μB and a static external magnetic field B, as . Spin vector precesses in the Bloch sphere around the axes of the applied static magnetic field (basis states axes) with so called Larmor frequency , where h is the Planck constant. For flipping the spin external oscillatory magnetic field BAC need to be apply perpendicular to the static one and its frequency need to match Larmor frequency. Reason for necessity to match the Larmour frequency can be explain using the kid swing example. Kid swing oscillates with its natural frequency of oscillation. If the swing is pushed with an appropriate period of pushing pulses, amplitude of the oscillation will increase and at some point swing will flip. In this comparison a natural frequency of a kid swing correspond to a Larmor frequency and a frequency of pushing pulses to the frequency of the applied oscillatory magnetic field.

Oscillatory magnetic field is hard to implement, from the fabrication standpoint. One way to avoid this problem is to apply static instead of oscillatory magnetic field and to apply an oscillatory voltage to the quantum dot gate. Oscillatory electric field than modulates the hole g factor giving equivalent oscillatory magnetic field from the first case.

For generating high frequency signal, microwave sources are needed because of high Larmor frequencies (tens of gigahertz). For this purpose signal generator SMF100A from Rohde and Schwarz will be used, controlled also from the python measurement application.

Described technique for spin rotation is called electron-dipole spin resonance (EDSR) [11].

#### Measuring the spin dephasing time T2\*

Following the approach of R. Maurand et al., for evaluating inhomogeneous dephasing time T2\*, Ramsey – fringes like experiment will be conducted [11]. First, the EDSR ∏/2 (90⁰) pulse around x axes is applied to bring the spin vector from the z axes to the xy plane in Figure 10. It stays there for the time τ being exposed to the dephasing noise. After the time τ, ∏/2∆Φ pulse around axes which is x axes rotated for ∆Φ, will be applied to project the spin vector back on the z axes for the readout. Linear increase of the ∆Φ between the measurement points results in the sinusoidal oscillation of the measured spin up state probability. From its exponentially decaying envelope dephasing time T2\* can be extracted, according to [11].

#### The spin coherence time experiments:

##### Hahn echo T2

To exctract the instrinsic coherence time T2 mainly determined by the dominant dephasing source, Hahn – echo experiment will be conducted. Similar to the spin dephasing time measurement, after the first ∏/2 pulse around x axes spin vector lays in the xy plane. Because of the dephasing sources spin dephases in the xy plane for time τ. Then the ∏ pulse around the y axes will be applied which mirrors the spin vector around the y axes. The spin is then left to dephase for the same time, but since mirrored, the direction of this dephasing will cancel the previous one to a some degree, causing the spin refocusing. After that by the next ∏/2∆Φ pulse around axes which is x axes rotated for ∆Φ, spin is projected to z axes and a spin up probability is measured. From its exponentially decaying envelope in this case coherence time T2 will be extracted.

##### CPMG pulse sequence T2CPMG

The sequence of the ∏ pulses called the Carr-Purcell-Meiboom-Gill (CPMG) sequence, rotating the spin around the y axes can be applied at the times τ, 3τ, 5τ…, instead of the single ∏ pulse, as in the Hahn echo experiment, for the spin refocusing. Coherence time T2CPMG will be extracted from the exponentially decaying envelope of spin up probability vs ∏ pulses separation time τ (*I am not sure how it is actually measured*). This method is insensitive to the ∏ pulse errors, extending coherence time and it acts as a band pass filter, with the center frequency ωp = ∏/ τ, for the noise coupled to the qubit. By changing the ∏ pulses separation time τ adding more ∏ pulses, ωp can be shifted and the noise spectrum can be extracted [15].

### Innovative aspects:

In our group we are working with a **germanium nanowire based hole spin** double quantum dot. While other groups work with structures based on electron spin in gallium arsenide, electron spin in silicon and Si:P and hole spin in silicon, this particular approach is not yet investigated. It has promising theoretical proposals *(put in which proposals and some numbers maybe)* in terms of qubit spin state manipulation and coherence time. Easy and fast spin state manipulation is expected because of in situ present **large spin orbit coupling** for heavy holes in Ge which enable **fast spin manipulation** by applying oscillatory electric field to particular qubit gates (Figure 2) eliminating necessity for oscillatory magnetic field. This means reducing fabrication complexity because nothing else is required except of already defined gates. Together with all the fabrication reduction complexity brought by gate reflectometry (as explained in *Definition of the problem*) this approach has high chances of **addressing scalability issue**.

**Relatively long coherence time** is expected because of, before mentioned, low qubit charge spin coupling to the surrounding Ge and Si nuclei spin (**low hyperfine interaction**).

Gates in our DQD system (Figure 2) are positioned directly on the top of the nanowire in which quantum dots are formed. This implies **high capacitive coupling between gate and quantum dots**. This further implies **high sensitivity thus speed of gate reflectometry**, as explained in *Research methods (or work schedule)*.

### International collaboration:

We are collaborating with spin qubit team in **Charles M. Marcus** laboratory in Copenhagen, lead by **Ferdinand Kuemmeth**. Since they are mature group with a big knowledge in instrumentation and spin qubits in overall, this collaboration helps us a lot in setting up our measurement setup. It would be helpful to visit them several times throughout the year. Here I would like to ask for the finances to cover the trip and accommodation costs for that purpose. The other significant collaboration is with **J.J. Zhang** in Beijing, China. He is material scientist providing us with silicon germanium nanowire samples.

### Contingency plan:

In case it will be found out that the gate reflectometry technique does not work we are going to try to use a charge sensor ohmic reflectometry. (*maybe put some reasons why gate reflectometry should not work, but I don’t know what those can be*) For that reason a charge sensor proximate to the double quantum dot should be added to the nanofabrication process of our samples, similar to the approach used in [8], but replacing electrons with holes in our case. For the charge sensor a single hole transistor would be used in a form of a single quantum dot very close to the initial double quantum dot, thus capacitively coupled to it. Whenever charge configuration changes in the DQD, impedance of the charge sensor will change and thus reflected signal amplitude. *For the reflectometry on the single quantum dot, look the relfecotmetry principle description in the reflectometry explanation at the end of the “State of the art chapter”.*

*Such an approach is more mature in the community and thus it has bigger chances for success.*

### “Something about myself”

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THINGS THAT ARE KICKED OUT, BUT MAYBE SOME OF THOSE CAN BE IMPLEMENTED ABOVE:

*Measurements need to be sensitive enough to achieve a high enough signal to noise ratio (SNR) (typically SNR of more than 10) in a short time. Signal to noise ratio is the ratio of signal and noise amplitude in a given bandwidth. Measurement sensitivity is a measure of the change in an amplitude of current or amplitude (phase) of reflected wave when charge configuration is changed. Noise comes from 1/f noise on lower frequencies, intrinsic shot noise, thermal noise, noise in in measurement equipment… Lowering the measurement bandwidth (integration or filtering) noise is lowered and SNR raised but measurement become slower. Thus for achieving good SNR in short time signal need to be high. In our case fast measurement is required to obtain good quality measurement fast enough. (I think this part does not fit here, should be put when you explain how you will tune your reflectometry what is important)*

**Double quantum dot (DQD) (Use this part when you will describe your experiment in a DQD)**

For achieving good state preparation, fast manipulation and fast measurement, additional mechanisms are required beyond ones offered by single QDs. One of the most promising building block for the realization of the spin qubit quantum computer based on quantum dots is serial double quantum dot (DQD) system. A DQD system consists of two neighboring quantum dots tunnel coupled to each other, which simply means that they can exchange charge particles by tunneling. The



Figure 1: Spin state readout based on spin blockade in gate defined electron DQD. The blue circles represent the individual quantum dots, the grey lines the gates and the black arrows in the QDs the electron spin direction in the left and the right dot. In the case of two electrons on the right dot current through the charge sensor does not flow, otherwise it flows (NO!). I think you should not use here the charge sensor. Spin blockade can be observed also in a current measurement. I am afraid that the concepts are getting too much mixed.

main physical property which makes them favorable for the realization of a qubit is the Pauli exclusion principle. It says that two identical fermions (in this specific case electrons or holes) cannot occupy same energy state.

Figure 1 describes how spin blockade can be used to extract information about the electron spin in the left QD in the DQD system. If the spin configuration is like in Figure 1a) then after electrostatic pushing, by applying voltage pulses on gates L and R, electron is allowed to tunnel to the right dot, which, for example, can be detected as the DC current signal. In the other case, Figure 1c), electrons on both dots have same spin and due to Pauli exclusion principle they stay in that configuration after electrostatic pushing. Consequently, current DC current signal does not flow. (You need to speak about singlet triplet else it is not clear)

### Overall goal of the project:

To implement one of the Loss and DiVincenzo’s criteria:

* **strong quantum measurements**,

and conducting **experiments of spin manipulation**.

Strong quantum measurements can be achieved by implementing gate reflectometry in our type of qubit structures. After having state readout solved, spin manipulation experiments can be done by applying bursts of microwave signal on electrostatic gates *(as explained in research methods).*

Spin manipulation experiments will be guideline for achieving second of the Loss and DiVincenzo’s criteria:

* accurate quantum gate operations

## Specific aims

### Clear aims:

Samples are done in cleanroom… *(take from someone in group)*

All experiments are done on DQD and TQD samples placed on the printed circuit board (PCB) sample holder *(put the picture)* in the dilution refrigerator with a base temperature of 10 mK.



Fig. x1. PCB holder (green) with mounted nanowire based sample (middle, grey) fabricated in our group by Lada Vukušić. Altogether mounted on golden plated copper fork on the dilution fridge insert. Copper wires are coaxial cables providing high frequency connection for spin manipulation and readout. Nanometer gates and ohmic contacts on the sample are connected by wedge wire bonding.

Electrical connection with the sample is achieved through thermally low conductive looms for DC signals and coaxial cables for RF and microwave signals. *(put the picture of the probe)* All cables finish in PCB connector and further electrical contact with the sample is achieved by wedge wire bonding.

On room temperature side there are several instruments for sending and receiving the signals from the sample. Firstly, DQD and TQD needs to be tune in correct electrostatic configuration what is achieved through the low-noise, optically isolated, voltage DC sources.

Sequences of high-speed pulses (ranging from hundreds of nanoseconds to several milliseconds) coordinated together with bursts of microwave signals (several GHz up to several tens of GHz) are sent via coaxial cables to manipulate DQD and TQD charge and spin state thus **providing spin qubit manipulations**.

Pulses are generated by arbitrary waveform generator (Tektronix AWG5014C) and microwave signals by microwave signal source (Rohde & Schwarz SMF100A).

**Qubit state is read-out** by probing radio-frequency (RF) signal reflected from resonant circuit consisted of discrete inductor and capacitor and gate capacitance between DQD and TQD top gates and confined charge area in those. Probing is done by high frequency lock-in measurement technique using Zurich Instruments UHFLI lock-in amplifier.

### Hypoteses:

*(Don’t know what to put here and what in research metodology)*

Main hypotheses is that our gate reflectometry is sensitive enough to achieve fast quantum state readout. Read out parameter (one which needs to be boosted) by gate reflectometry is resonance frequency shift ∆f due to hole tunneling form one to another dot in DQD or TQD system: . Resonant frequency, , of resonance circuit depend on externally added lumped inductance L which is externally added, and parasitic capacitance Cp. Because L is easily tunable and Cp can be reduced to some level by engineering, main hypotheses is that quantum capacitance due to a hole tunneling, CQ is big. It is given by our sample and we expect it to be relatively high because of the following reasons.

*(This need to be changed according to Csigma)*

CQ depends on capacitive coupling of reflectometry readout gate to QDs in a qubit Cg, and parasitic capacitances Cp, according to:

Previous expression suggest that pathway for boosting sensitivity of gate reflectometry is to have Cg high and Cp low.

Since in our types of structures gates are positioned on the top of the nanowire (d is small, l and w are relatively large) consisting QDs (Fig 1.) we expect high Cg ,according to:

Small parasitic capacitance we are going to achieve by engineering our sample holder (PCB). Isolating PCB sample area from the ground by removing ground planes and decoupling RF and DC ground by putting relatively large resistors in DC line around that area. On Fig.x.1. around the sample PCB is translucent indicating that there is no copper ground plane.



Figure 1. Nanowire based single quantum dot, predecessor of double quantum dot on Fig.x.

## Research methods

Here we are proposing integration of two qubit Loss and DiVincenzo’s criteria in our type of qubit. First is **qubit state (spin) readout**. Other one is **spin state manipulation**.

### Qubit state readout:

C:\Users\jkukucka\Desktop\IST\DOC Fellowship\DQD_reflectometry.tif

Figure 2. Gate reflectometry schematic on the DQD sample from Fig.x1. LC resonators are connected to three of the gates. Signal from different gates are distinguished by frequency multiplexing since resonant frequencies are different because of different inductor values.

**What is reflectometry?**

Reflectometry is readout technique based on change of wave reflection coefficient Γ. It comes from electromagnetic wave principle – if the wave is travelling in media with impedance Z0  (e.g. coax cable) and it encounters change of impedance (e.g. coax end) to Z, portion of the wave will be reflected back according to the expression: , where Ar is amplitude and ᵠ( Ar) phase of the reflected, and Ain amplitude and ᵠ(Ain) phase of incoming wave. Reflection coefficient phase is ᵠ(Γ).

Putting resonant circuit with incorporated device instead of coax cable end one can measure change in impedance (capacitance) of that device. If elements of a resonant circuit – inductance L and capacitance C are properly chosen, on the resonant frequency of that circuit, , wave reflection coefficient Γ is minimized and it’s phase has inflection point and highest slope, Fig 2. top right blue and red.

In case of resonant LC circuit consisted of just L and C with very small R, Z is almost purely imaginary consisting of inductive and capacitive reactance. Thus if capacitance of sensed device changes -> ᵠ(Γ) changes and so phase of reflected wave ᵠ( Ar). Thus, by measuring phase of reflected wave ᵠ( Ar) and comparing it with ᵠ(Ain) one can get information of the impedance (capacitance) of sensed device.



Fig 3. S11 parameter vs frequency for different capacitors *(put something from qucs instead of this one)*

**Our plan:**

RF wave (tens to hundreds of MHz) is generated and sent from UHFLI out port down the coax cable. Going through directional coupler and encountering three resonant circuit frequency multiplexed on different resonance frequencies by choosing different values for surface mount inductors L1, L2, L3. Each of this inductors will be wire bonded to finger like gates, as shown in Fig 2. Here is an example for nanowire, double quantum dot based qubit. Gates LP (left plunger) and RP (right plunger) are capacitively coupled to the left and right quantum dot respectively. When electron undergo tunneling between the dots there is an onset of quantum capacitance, changing overall capacitance seen by the resonant circuit, which changes resonance frequency (according to expression for f0) and consequently amplitude and phase of reflected wave which is then measured.

### Spin state manipulation:

*Write something about it*

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